A low-power fast transient output capacitor-free adaptively biased LDO based on slew rate enhancement for SoC applications

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A B S T R A C T

In this paper, a highly efficient and fast transient output capacitor-free low-dropout regulator (LDO) presented. The proposed LDO architecture is based on differential transconductance amplifiers pairing with push–pull stage to enable effective output driving capability. The slew rate at the gate of the output transistor (SRG) is further enhanced by common mode-feedback (CMFB) resistors and a coupling capacitor to bypass band-limited components. By adopting adaptive biasing (ADB) technique, the loop bandwidth is extended proportionally to the output load while maintaining high current efficiency at minimum load. The proposed LDO is designed using cost-effective 0.35 μm CMOS technology. Post-layout simulation results show that the LDO occupies an active area of 0.069 mm², consuming only a quiescent current of 4.45 μA at a minimum load of 100 μA. The LDO is able to regulate the output at constant 1.2 V with a dropout voltage of 0.2 V. When the load is ramped from 100 μA to 100 mA in 100 ns, the output transient can be fully recovered within 2 μs.

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1. Introduction

Low-dropout regulators (LDOs) are one of the most essential module in modern power management integrated circuits (PMICs), supplying clean and ideally ripple-free supply voltage to noise sensitive blocks such as analogue, mixed-signals or high-frequency circuit blocks [1–4]. As illustrated in Fig. 1, Li-ion batteries normally fluctuate between 4.2 V (fully charged) and 3.7 V upon complete discharge. Switching regulator is often used as a pre-regulators due to their high conversion efficiency but they introduce unwanted harmonics. Therefore, LDOs are used as post-regulators in order to reject the harmonic ripples effectively [5].

Recent development of highly integrated System-on-Chip (SoC) design leads to the production of more powerful consumer electronics products such as smartphones, requiring several LDOs in order to optimise the power consumption of different circuit blocks independently, thereby improving the system performance [6]. More importantly, realisation of SoC requires the LDOs to operate without relying on off-chip capacitors to reduce power-line distance and cross-talks, resistive and inductive parasitic due to bond wires and I/O pads, thereby cutting down printed circuit board (PCB) area and hence cost saving can be achieved [5,7–10].

For portable handheld devices, efficiency is a critical key in extending the battery life [10–12]. This can be achieved by lowering down the quiescent current (IQ) and dropout voltage (VDO). However, output capacitor-free LDOs suffer from the trade-off between efficiency and transient performance. By referring to Fig. 2a, low IQ unavoidably reduces the loop bandwidth and the slew rate at the gate of Mpass (SRG) owing to its large gate capacitance (CG) [6,12], where SRG is defined by [13]

\[
SRG = \frac{IQ}{CG} = \frac{V_G}{dt}
\]  

(1)

For Mpass to route the same amount of current, VDO can be further reduced by increasing its width as illustrated in Fig. 2b [12]. Since CG is proportional to the transistor size, SRG is further reduced, increasing the time taken to charge up or discharge CG. Therefore, the output transient response is severely affected.

Several techniques have been proposed over the past few years. The LDO architecture reported in [14] achieved a fast transient by consuming relatively high IQ of 6 mA, stabilised by a large 0.6 nF on-chip capacitor. However, this approach degrades the current efficiency (ηC) at light loads as well as occupying large chip area, which is not preferred for low power design and area-limited SoC. In [6,15–16], a simple yet area efficient LDO architecture based on flipped–voltage follower (FVF) is proposed. However, this results in poor regulating accuracy due to low loop gain, although stability...
can be achieved without additional compensating capacitor. The modified FVF reported in [17] adopted 4 stacking cascaded transistors to achieve precise regulation (high gain) but it requires a larger voltage headroom which is not suitable for low-voltage applications these days. Therefore, it is very challenging to design an LDO fulfilling all the performance parameters.

This paper presents a highly current efficient and fast transient LDO based on differential transconductance amplifier, in which SRc is further enhanced by a pair of CMFB resistors and a high pass coupling capacitor. The working principles and schematic implementation of the proposed architecture are presented in Section 2. Then, the large signal and stability analysis are presented in Sections 3 and 4 respectively. Subsequently, post-layout simulation results are shown in Section 5. Finally, conclusion is drawn in Section 6.

2. Proposed LDO architecture

2.1. Concept

The concept of the proposed LDO architecture is illustrated in Fig. 3. The architecture consists of a differential transconductance amplifier (Gm) pair - GmH and GmL, a reference buffer, a pair of CMFB resistors, push–pull summation circuit, coupling capacitor (Cp) and an adaptive biasing circuit. The output voltage of the LDO (Vout) and reference buffer are set to be equivalent in steady state. These circuits are connected to the inputs of the Gm pair with opposite polarity. The function of Gm pair is to momentarily sense and convert the input differential voltage \( V_{id} = |V_{out} - V_{ref'}| \) into current whenever there is a large change in output current \( (\Delta I_{out}) \), causing Vout to undershoot and overshoot respectively. The generated current is then increased by the CMFB resistors by 2nd order and goes through a push–pull summation circuit for charging up and discharging the gate capacitance of the output transistor \( M_{pass} \). The reference buffer is used to drive the Gm pair from \( V_{ref} \) generated from the bandgap reference.

When the LDO draws heavy load, smaller size of \( M_{pass} \) can be allowed to operate in triode region to reduce chip area [18]. However, the sensitivity of the \( I_{out} \) with respect to the source-gate voltage \( (V_{SC}) \) of \( M_{pass} \) is reduced. Therefore, higher bandwidth and SRc are mandatory at heavy load for the gate capacitance of \( M_{pass} \) to be charged up and discharged. This is done by adopting an ADB technique such that \( I_{3} \) is made directly proportional to the output current \( (I_{out}) \). Unfortunately, the time taken for ADB to activate when the load ramps up does not reflect its effectiveness due to band-limited circuit components such as \( G_{ML} \) and \( G_{MH} \). In order to minimise the dependence of transient response on the bandwidth as well as to reduce the Vout spike, coupling capacitor \( (C_p) \) is used to counteract these problem, bypassing \( G_{ML} \) and \( G_{MH} \) by capacitive coupling.

2.2. Schematic implementation

The schematic of the proposed LDO is shown in Fig. 4. The \( G_{ML} \) and \( G_{MH} \) are made up of transistors \( M_1, M_2, M_3 \) and \( M_4, M_5, M_6 \) respectively in the form of differential–input common gate amplifiers. The CMFB resistors \( (R_{FB}) \) are connected between the drain terminal of transistors \( M_{12} - M_{13} \) respectively and their gate terminal, thus sharing the same gate voltage. To enable effective push–pull ability in charging up and discharging the gate capacitance of \( M_{pass} \), push–pull current mirror is employed to drive the \( M_{pass} \), realised by transistors \( M_{13} - M_{14} \) and \( M_{11} - M_{12} \). Transistors \( M_{14} - M_{12} \) act as a cascoding stage to increase the DC gain of the LDO for more accurate and precise regulation, as 3 stacked cascaded transistors are feasible for low-voltage design, i.e. \( V_{nom} = 1.2 \) V [8–9,18]. The ADB circuit is implemented by area efficient current mirrors, realised by \( M_{17} - M_{18} \). Besides that, on-chip metal line for power transfer and input capacitance of the functional for \( G_{FB} \) pairs by sensing the \( V_{out} \) spikes directly to the push–pull pair and its value is selected to be 1 pF. Effective pole splitting is done by Miller Compensating capacitor \( C_C \) with 4 pF to ensure sufficient phase margin (PM) when \( I_{out} \) is low.

Reference buffer is realised by 2-stage operational amplifier with unity gain feedback, constructed by transistors \( M_7 - M_9 \). Compensation is not necessary because \( V_{ref} \) is relatively stable such that the slew rate is not a concern to affect the performance of the LDO [12]. Nevertheless, \( M_7 \) it is a critical component to source sufficient instantaneous current when \( V_{out} \) overshoot or undershoot occurs. If the size of \( M_7 \) is too small, more \( V_{SG} \) will be dropped across \( M_7 \), resulting in inaccurate voltage regulation. If size of \( M_7 \) is too large, parasitic capacitance increases and hence transient performance is affected.

In the event when \( I_{out} \) ramps down from maximum to minimum, causing \( V_{out} \) to overshoot, more drain current of \( M_7 \) (\( I_{out} \)) is generated due to non-inverting common gate configuration from \( V_{out} \) to \( V_{GHz} \) and \( I_1 \) is reduced due to inverting configuration from node \( V_{out} \) to \( V_L \). As such, lesser current is mirrored to \( M_4 \), and larger amount of current is mirrored to \( M_{15} \) and then \( M_{16} \) simultaneously. The gate of \( M_{pass} \) is then charged up by the momentarily increased current, increasing its gate-source voltage \( (V_{GSPass}) \) so that \( V_{out} \) transient can be recovered.

Similarly, when \( I_{out} \) ramps up from minimum to maximum, \( V_{out} \) undershoots such that the magnitude of \( I_l \) and \( I_l \) changes...
oppositely so that more current is mirrored to \( M_{14} \), thereby providing a quick discharging path for the gate of \( M_{pass} \) to pull down \( V_x \) so that \( V_{out} \) can be regulated back to desired value. The effect of CMFB resistors, \( C_p \) will be demonstrated with mathematical analysis in the next section.

### 3. Large signal analysis

#### 3.1. \( G_M \) pair

The extracted \( G_M \) pair is illustrated in Fig. 5. \( G_M \) is defined as the rate of change of \( I_L \) or \( I_H \) with respect to \( V_{id} \) as mentioned earlier, i.e.

\[
G_{bi} = \frac{\partial I_{bi}}{\partial V_{id}}
\]

(2)

Thus, when \( V_{out} \) overshoot occurs, \( G_{bi} \) is momentarily changed by

\[
G_{ML} = \beta_L \left(-V_{id} + \frac{g_{mL}}{\beta_B}\right)
\]

(3a)

\[
G_{MH} = \beta_H \left(V_{id} - \frac{g_{mH}}{\beta_B}\right)
\]

(3b)

Where \( \beta \) is the transconductance parameters, defined by

\[
\beta = \mu C_{ox} \frac{W}{L}
\]

(4)

and \( g_{mx} \) is the transconductance of the transistor \( x \), generally defined by

\[
g_{mx} = \sqrt{2\beta_x(I_B + I_{AB})}
\]

(5)

The sign of \( V_{id} \) interchanges in (3a) and (3b) when \( V_{out} \) undershoots, indicating the complementary action by the \( G_M \) pair. Since \( I_{LH} = I_B + I_{AB} \) provided that the ratio of the 2 current mirror pairs \( M_1 : M_8 \) and \( M_{16} : M_{9} = 1 : 1 \), \( G_M \) and \( G_MH \) also increase with \( I_{AB} \) which increases with \( I_{out} \).

#### 3.2. Coupling capacitor

When \( V_{out} \) spike is detected by \( C_p \), the gate voltage of \( M_{15} \) is momentarily charged up by capacitive coupling, thus pulling more transient current. Then, the total drain current of \( M_{15} \) is given by

\[
l_{M15} + \Delta I_{M15} = \frac{\beta_{15}}{2} (V_{GS15} + \Delta V_{GS15} - V_{TH})^2
\]

### 3.3. CMFB resisters

The analysis of CMFB resistors is illustrated in Fig. 6. Suppose when \( V_{out} \) overshoots, output current of \( G_M \) and \( G_MH \), \( I_L \) and \( I_H \) respectively can be defined by

\[
l_L = \frac{\beta_L}{2} \left(-V_{id} + \sqrt{\frac{2(I_B + I_{AB})}{\beta_B}}\right)^2
\]

(8a)

\[
l_H = \frac{\beta_H}{2} \left(V_{id} + \sqrt{\frac{2(I_B + I_{AB})}{\beta_B}}\right)^2
\]

(8b)
With the absence of $R_{FB}$, the charging current $I_C$ can be found as

$$I_C = \frac{I_{16}}{C_0} I_{14} \quad \text{or} \quad I_C = 4\beta H V_{id} \sqrt{2(l_B + l_{AB}) \beta_{8,9}}$$

indicating that $I_C$ is a linear function of $V_{id}$. Now, with the introduction of $R_{FB}$, the differential current $I_D = I_H - I_L$ is now sensed by $R_{FB}$ and the current flowing through it is given by $I_{RFB} = (I_H - I_L)/2$. Since the matched $M_{12}$ and $M_{13}$ share the same gate voltage $V_{gcm}$, they have the same common drain current $I_{CM}$, defined by $I_{CM} = (I_H + I_L)/2$ or

$$I_{CM} = \frac{\beta H L}{2} \left[ V_{id}^2 + \frac{2(l_B + l_{AB})}{\beta_{8,9}} \right]$$

Therefore, the $I_C$ now can be easily found as

$$I_C = 4\beta_{14,16} H^2 V_{id} R_{FB} \sqrt{\frac{2(l_B + l_{AB})}{\beta_{12,13} \beta_{8,9}}} V_{id} + \sqrt{\frac{2(l_B + l_{AB})}{\beta_{8,9}}}$$

Based on (11) above, it is obvious that $I_C$ is a dependent quadratic function of $V_{id}$, showing that same factor of increment in $V_{id}$ results in higher amount of $I_C$ compared to the linear relation in (9), thereby enhancing the SR of quicker recovery time of $V_{out}$. It is also evident that the width of $M_8$, $M_9$, $M_{12}$ and $M_{13}$ can be reduced to further increase $I_C$.

4. Stability analysis

Referring to [18], LDO with ADB technique comprises of 2 inherent feedback loop in the circuit, namely the main regulating (MRG) loop and the adaptive biasing (ADB) loop.
4.1. MRG loop

The small signal model of the proposed LDO is shown in Fig. 7. The loop is broken at node $v_{out}$. The relationship between $v_m$ and $v_1$, $v_H$ forms an inverting and non-inverting configuration respectively. In the event when $v_m$ is positive, $v_H$ increases and $v_L$ decreases. As a result, the drain current of $M_{15}$ is $g_{m15}v_H$, mirrored to $M_{16}$ to charge up the gate of $M_{pass}$, thus increasing $v_g$ so that $v_{out}$ can be revived from overshoot. Meanwhile, current $i_p$, given by $sC_p(v_{out} - v_H)$, is also injected into the gate of $M_{15}$, further increasing $v_H$ at a faster rate. The transfer function is derived as shown in (12) by adopting the following assumptions into consideration: (i) transistors $M_L$ and $M_H$ are matched such that $g_{mL} = g_{mH} = G_m$, (ii) transistors in push–pull current mirror pairs are matched such that $g_{m14} = g_{m15} = g_m$, (iii) $C_1$ and $C_2$ are too small that can be omitted, (iv) $C_X = C_g + C_C$ and (v) output capacitance $C_{out}$ is much larger than $C_g$, $C_C$ and $C_P$. 

Fig. 12. Frequency response of the ADB loop at different loading conditions.

![Frequency response of the ADB loop at different loading conditions.](image1)

![Small signal model of the ADB loop.](image2)

![Complete layout of the proposed LDO and (b) close up view of the control circuits.](image3)
The output impedance is defined as $R_{out} = \frac{R_{load}}{1/G_{mil}}$, where $R_{load}$ is the effective input impedance of the load. Due to the term $1/G_{mil}$, $R_{out}$ is very small such that it resembles the characteristics of an ideal regulator in which a large increase in $I_{out}$ causes a small change in $V_{out}$. On the other hand, the gate resistance $R_g$ is increased tremendously by $g_{mC}f_{AC}$ due to cascading configuration, where $R_g = \frac{f_{AC}t}{g_{mC}t_{AC}}$. DC gain ($A_{DC}$) and dominant pole ($p_{-3db}$) are given respectively by

$$A_{DC} = \frac{g_{mR}g_{mpRFB}R_{FB}R_{out}}{G_{mil}}$$

$$p_{-3db} = -\frac{1}{R_g}\left(G_{mil} + g_{mpRout}C_{C}\right)$$

In order to balance the trade-off between the $C_g$ and $R_g$ such that both $A_{DC}$ and $p_{-3db}$ corresponding to regulating accuracy and transient response respectively are not compromised, $M_{pass}$ is designed at minimum channel length $L_{min} = 0.35 \mu m$ while the channel length of the rest of the transistors are set to be $0.5 \mu m$. The aspect ratio of the transistors are summarised in Table 1.

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{2g_{m}G_{mil}g_{mpRFB}R_{FB}R_{out}}{C_g + g_{mpRout}C_{C}}\left(1 + \frac{R_gC_g}{C_g + g_{mpRout}C_{C}}\right)\left[1 + \frac{sR_gC_g}{C_g + g_{mpRout}C_{C}} + \frac{g_{mpRout}C_{C}}{C_g + g_{mpRout}C_{C}}\right]$$

By assuming single pole transfer characteristics, the unity gain frequency, $\omega_{UGF}$ can be approximated as

$$\omega_{UGF} = \frac{2g_{m}G_{mil}g_{mpRFB}R_{FB}R_{out}}{C_g + g_{mpRout}C_{C}}$$

Due to the effect of ADB, the bandwidth, or $\omega_{UGF}$ of the LDO is also extended in proportion to $I_{out}$ due to increased $g_{m}, G_{mil}$ and $g_{mp}$. The improvement of $\omega_{UGF}$ can be seen from the frequency response of the MRG loop as shown in Fig. 8. Besides that, a pair of non-dominant complex poles exists, exhibited by magnitude peaking determined by Q-factor. Non-dominant complex poles pair $[p_{23}]$ and Q-factor are approximated as

$$|p_{23}| = \sqrt{\frac{C_g}{R_{FB}R_{out}C_P(C_gC_C + C_gC_{C})}}$$

$$Q \approx \frac{\sqrt{R_{FB}R_{out}C_P\left(C_gC_C + C_gC_{C}\right)}}{R_{FB}C_P}$$

Although magnitude peaking causes abrupt change in phase therefore causing instability for the LDO, this is only true when the peaking occurs near $\omega_{UGF}$. As shown in Fig. 8, the peaking occurs far beyond $\omega_{UGF}$ due to low $R_{out}$ in the denominator of (15). Thus, stability issue is not affected [19] and Q-reduction capacitor is not necessary. Based on (17), the Q factor is relatively constant throughout the full range of load due to the absence of $g_{mp}$. The Q factor is able to maintain well below 0.92 across the allowable range of $I_{out}$ as illustrated in Fig. 9 below. Since the gain margin (GM) is inversely proportional to Q factor, approximated as

$$\text{GM} \approx 20 \log \left(\frac{|p_{23}|}{Q\omega_{UGF}}\right)$$

Therefore, GM is also well kept above safety margins ($\geq 10$ dB) across the allowable range of $I_{out}$ as shown in Fig. 10.

There are 2 zeros, a left-half-plane (LHP) and a right-half-plane (RHP) zero, defined respectively by

$$z_1 = -\frac{2R_{FB}C_P - 2\xi}{s\omega_0}$$

$$z_2 = \frac{g_{m}R_{FB} - 2C_{C}}{R_{FB}C_{C} + \frac{\xi\omega_0}{s\omega_0}}$$

Since non-dominant complex poles exist, PM can be approximated as

$$\text{PM} \approx 90^\circ - \tan^{-1}\left(\frac{\omega_{UGF}}{Q|p_{23}|\left[1 - (\omega_{UGF}/|p_{23}|)^2\right]}\right) + \frac{\tan^{-1}(\omega_{UGF}/z_1)}{z_1}$$
4.2. ADB loop

The small signal model of ADB loop is shown in Fig. 11. According to [18], both MRG loop and ADB loop must be stable to guarantee the stability of the LDO. As shown in (12), the MRG loop is a negative feedback system characterised by its negative sign for the DC gain, and the stability is determined by its PM. Nevertheless, the stability of the ADB loop is determined by the types of its feedback transfer action. Hence, instead of investigating the complete transfer function, the magnitude of the DC gain will be derived. The ADB technique adopted by [18] is a positive feedback system, in which the magnitude of the DC gain is much lesser than unity to guarantee stability. However, the ADB scheme of the proposed LDO is negative feedback in nature, in which its gain must be much greater than unity, shown by

$$|\text{ADB(ABL)}| = \frac{g_{mab1}}{g_{mab2}} \left( \frac{1 - \frac{g_{mab}}{g_{mp}} GM_{\text{Rout}}}{g_{mp} GM_{\text{Rout}}} \right)$$

(22)

### Table 2

Post-layout simulation results for different process corners and temperature.

<table>
<thead>
<tr>
<th>Corner</th>
<th>$V_{\text{out}(100,\mu\text{A})}$ (V)</th>
<th>$V_{\text{out}(100,\text{mA})}$ (V)</th>
<th>$\Delta V_{\text{OS}}$ (mV)</th>
<th>$t_{\text{OS}}$ (µs)</th>
<th>$\Delta V_{\text{US}}$ (mV)</th>
<th>$t_{\text{US}}$ (µs)</th>
<th>PM$_{100,\mu\text{A}}$ (%)</th>
<th>PM$_{100,\text{mA}}$ (%)</th>
<th>GM$_{100,\mu\text{A}}$ (dB)</th>
<th>GM$_{100,\text{mA}}$ (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>All best</td>
<td>25-25</td>
<td>1.198</td>
<td>1.190</td>
<td>0.81</td>
<td>92</td>
<td>1.70</td>
<td>58</td>
<td>61</td>
<td>53.4</td>
<td>25.9</td>
</tr>
<tr>
<td>All best</td>
<td>27-27</td>
<td>1.201</td>
<td>1.198</td>
<td>0.85</td>
<td>105</td>
<td>1.82</td>
<td>56.9</td>
<td>59.3</td>
<td>52</td>
<td>25</td>
</tr>
<tr>
<td>All best</td>
<td>100-100</td>
<td>1.204</td>
<td>1.398</td>
<td>0.93</td>
<td>139</td>
<td>1.96</td>
<td>55.2</td>
<td>55.2</td>
<td>50.3</td>
<td>22</td>
</tr>
<tr>
<td>All typical</td>
<td>25-25</td>
<td>1.196</td>
<td>1.92</td>
<td>0.9</td>
<td>107</td>
<td>1.87</td>
<td>55.6</td>
<td>57.6</td>
<td>51.2</td>
<td>23.4</td>
</tr>
<tr>
<td>All typical</td>
<td>27-27</td>
<td>1.202</td>
<td>1.195</td>
<td>0.94</td>
<td>100</td>
<td>1.95</td>
<td>55</td>
<td>55</td>
<td>50</td>
<td>20.3</td>
</tr>
<tr>
<td>All typical</td>
<td>100-100</td>
<td>1.205</td>
<td>1.198</td>
<td>1.08</td>
<td>139</td>
<td>2.11</td>
<td>54.1</td>
<td>53.7</td>
<td>48.8</td>
<td>19.2</td>
</tr>
<tr>
<td>All worst</td>
<td>25-25</td>
<td>1.195</td>
<td>1.189</td>
<td>1.04</td>
<td>131</td>
<td>1.93</td>
<td>54.6</td>
<td>54.4</td>
<td>49.8</td>
<td>26</td>
</tr>
<tr>
<td>All worst</td>
<td>27-27</td>
<td>1.198</td>
<td>1.192</td>
<td>1.14</td>
<td>142</td>
<td>2.24</td>
<td>53.2</td>
<td>51.2</td>
<td>49</td>
<td>25</td>
</tr>
<tr>
<td>All worst</td>
<td>100-100</td>
<td>1.202</td>
<td>1.189</td>
<td>1.27</td>
<td>151</td>
<td>2.49</td>
<td>52.5</td>
<td>49.8</td>
<td>47</td>
<td>21.1</td>
</tr>
</tbody>
</table>

Fig. 16. PSR against frequency at different loading conditions.

![Fig. 16](image1)

![Fig. 17](image2)

Fig. 17. (a) Comparison of load transient response with and without $R_{FB}$ and (b) slewing current at the gate of $M_{\text{pass}}$ with and without $R_{FB}$.
From (22) above, it is evident that since $R_{out}$ is very small and $\delta_{ma(2)}$ can be made smaller by decreasing its width, $|\Delta_{DC(ADB)}|$ will be much greater than unity. As shown in Fig. 12, the DC gain of the ADB loop at $I_{out}$ of 100 $\mu$A, 1 mA, 10 mA, 100 mA are 27.8 dB, 28 dB, 27.3 dB and 21 dB respectively. Besides that, by comparing Figs. 8 and 12, $\omega_{UGF}$ of the ADB loop at each loading condition is higher than the MRG loop. This makes the LDO to be less dependent on the bandwidth of the MRG loop in a response to the change in $I_{out}$, thus extending the bandwidth of the LDO.

5. Post-layout simulation results

The proposed LDO is designed and simulated using MIMOS 0.35 $\mu$m CMOS process. The LDO is capable of providing a stable load ranging from 100 $\mu$A to 100 mA while regulating the output at 1.2 V. The designed LDO occupies an active area of 0.069 mm$^2$ as shown in Fig. 13(a). A close up view of the layout of the control circuits is also shown in Fig. 13(b).

The simulated consumed quiescent current $I_Q$ against output current $I_{out}$ and $\eta_C$ against output current $I_{out}$ are shown in Fig. 14 (a) and (b) respectively. The total consumed $I_Q$ at minimum load is only 4.45 $\mu$A. By comparing the proposed LDO with ADB and without ADB, although the $I_Q$ increases up to 0.13 mA at full load, $\eta_C$ is maintained well above 99%. Besides that, $\omega_{UGF}$ can from several hundreds of kHz up to 7.3 MHz even though there is only a negligible deterioration in $\eta_C$ of less than 0.2% at full load as shown in Fig. 14(c).

On the other hand, the load transient at boundary condition is simulated as shown in Fig. 15 such that $I_{out}$ is stepped between 100 $\mu$A (minimum load) and 100 mA (maximum load) in 5 $\mu$s with a rise and fall time of 100 ns under the following condition, i.e., $C_{out} = 100$ pF and $V_in = 1.4$ V. The proposed LDO is able to settle in less than 2 $\mu$s with 125 mV and 100 mV of undershoot and overshoot respectively. However, the difference in settling time and voltage spikes for undershoot ($\Delta V_{US}$) and overshoot ($\Delta V_{OS}$) is due to different RC time constant in charging and discharging sourcing current (shown in Fig. 6) for charging process when $V_{out}$ overshoots has longer RC time constant due to larger impedance. Hence, the instantaneous current drawn to charge up the gate of $M_{pass}$ is lower in overcoming $\Delta V_{OS}$ than the current for $\Delta V_{US}$.

The power supply rejection (PSR) of the LDO is simulated at $I_{out}$ of 100 $\mu$A, 1 mA, 10 mA and 100 mA and the result is shown in Fig. 16. As PSR performance at DC/low frequency is inversely proportional the loop gain [5,20], The designed LDO achieved the best PSR result at low frequency when $I_{out}$ is 10 mA at about –67 dB at 100 Hz, –62 dB at 1 kHz, and it starts to deteriorate beyond $f_{3dB}$ to –45 dB at 10 kHz and –6 dB at 100 kHz. At full load of 100 mA, the PSR at DC/low frequency degrades to –30 dB.

Fig. 18. PM against $I_{out}$ at different $R_{FB}$.

Fig. 19. Load transient of the proposed LDO at (a) $R_{FB} = 10$ k$\Omega$ and (b) $R_{FB} = 50$ k$\Omega$.

Fig. 20. Load transient of the proposed LDO with and without $C_C$ and ADB.
because $M_{\text{pass}}$ is operating in triode region. However, the range is extended up to 10 kHz because $I_Q$ is increased at full load by ADB, thereby pushing $p_{\text{4dB}}$ at higher frequency.

Subsequently, load transient simulations of different process corners and temperatures have been performed to guarantee the robustness of the proposed LDO. The result is tabulated in Table 2 where $V_{\text{out(min)}}$ and $V_{\text{out(max)}}$ are the output regulated voltage at minimum and full load, $\Delta V_{\text{US}}$ and $\Delta V_{\text{OS}}$ are voltage undershoot and overshoot respectively and finally $t_{\text{US}}$ and $t_{\text{OS}}$ are undershoot and overshoot settling time respectively. The effectiveness of CMFB resistors pair in enhancing $SR_C$ at the gate of $M_{\text{pass}}$ is also demonstrated via load transient response and $SR_R$ as shown in Fig. 17. It is obvious that the addition of $R_{FB}$ improves the $SR$ compared to the absence of $R_{FB}$. As a result, the transient voltage spikes are reduced significantly.

Nevertheless, it has been revealed that the $R_{FB}$ exhibits a trade-off between $SR_C$, PM and $A_{\text{FB}}$ for precise regulation. According to (11) and (13), a larger $R_{FB}$ improves the $SR_R$ as well as regulating accuracy. However, this pushes the complex poles $p_{\text{23}}$ to a lower frequency as proved in (16), degrading the PM throughout the allowable range of load current, thus the circuit may lead to shoot and overshoot settling time respectively.

Table 2 Performance comparison between recently developed LDOs.

<table>
<thead>
<tr>
<th>Work</th>
<th>[4]</th>
<th>[7]</th>
<th>[16]</th>
<th>[23]</th>
<th>[24]</th>
<th>[25]</th>
<th>[26]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tech. (μm)</td>
<td>0.13</td>
<td>0.18</td>
<td>0.065</td>
<td>0.18</td>
<td>0.18</td>
<td>0.18</td>
<td>0.065</td>
<td>0.065</td>
</tr>
<tr>
<td>$V_{\text{in}}$ (V)</td>
<td>1.4</td>
<td>1.4</td>
<td>1.2</td>
<td>1.2</td>
<td>1.4</td>
<td>1.2</td>
<td>1.2</td>
<td>0.75</td>
</tr>
<tr>
<td>$V_{\text{out}}$ (V)</td>
<td>2</td>
<td>1.2</td>
<td>1.0</td>
<td>1.0</td>
<td>1.2</td>
<td>1.0</td>
<td>1.0</td>
<td>0.5</td>
</tr>
<tr>
<td>$V_{\text{IO}}$ (mV)</td>
<td>200</td>
<td>200</td>
<td>200</td>
<td>200</td>
<td>200</td>
<td>200</td>
<td>200</td>
<td>200</td>
</tr>
<tr>
<td>$I_{\text{OUT}}$ (mA)</td>
<td>1.18</td>
<td>0.55</td>
<td>82</td>
<td>330</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$t_{\text{OUT}}$ (mA)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>$I_{\text{Q}}$ (mA)</td>
<td>4.1</td>
<td>46.4</td>
<td>51.7</td>
<td>50-90</td>
<td>14-53.5</td>
<td>40</td>
<td>3.7</td>
<td>27.5-68</td>
</tr>
<tr>
<td>$C_{\text{in}}$ (capcitance) (pF)</td>
<td>4</td>
<td>2.5</td>
<td>7</td>
<td>10</td>
<td>0</td>
<td>0.2</td>
<td>8</td>
<td>2</td>
</tr>
<tr>
<td>$C_{\text{out}}$ (pF)</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>$n_f$</td>
<td>96.06, 99.99</td>
<td>N/A, 99.95</td>
<td>N/A, 99.95</td>
<td>N/A, 99.95</td>
<td>96.15, 99.96</td>
<td>67, 99.96</td>
<td>67, 99.96</td>
<td>67, 99.96</td>
</tr>
<tr>
<td>$t_R$ (μs)</td>
<td>~1.16</td>
<td>~7</td>
<td>~0.0115</td>
<td>~3.96</td>
<td>~3.17</td>
<td>~6</td>
<td>~0.2</td>
<td>~1.65</td>
</tr>
<tr>
<td>Active area (m²)</td>
<td>500</td>
<td>400</td>
<td>0.2</td>
<td>200</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>Edge time (ns)</td>
<td>2500</td>
<td>2000</td>
<td>1</td>
<td>1000</td>
<td>500</td>
<td>5000</td>
<td>500</td>
<td>500</td>
</tr>
<tr>
<td>K</td>
<td>0.095</td>
<td>3.248</td>
<td>0.00575</td>
<td>0.55</td>
<td>0.468</td>
<td>0.222</td>
<td>0.11</td>
<td>0.782</td>
</tr>
<tr>
<td>F.O.M.1 (ns)</td>
<td>40.7</td>
<td>50</td>
<td>0.41</td>
<td>46</td>
<td>15</td>
<td>51</td>
<td>4.8</td>
<td>9</td>
</tr>
<tr>
<td>F.O.M.2 (mV)</td>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* Simulation results.
* Experimental results.
* Estimated from figure.

where $T_s$ is the settling time, $I_Q$ is the quiescent current and $I_{\text{MAX}}$ is the maximum load current, $\Delta V_{\text{OUT}}$ is the maximum change in $V_{\text{OUT}}$ and $K$ is the edge time ratio, defined by

$$K = \frac{\text{smaller} \times \text{rise/fall}}{\text{among designs for comparison}}$$

F.O.M.1 determines the transient performance in terms of settling time. Besides that, since the rise/fall time of $I_{\text{OUT}}$ is also a critical factor affecting $\Delta V_{\text{OUT}}$, F.O.M.2 is used for normalisation with reference to the smallest rise/fall time among the comparisons to determine the transient performance in terms of $\Delta V_{\text{OUT}}$, in which a lower F.O.M.1, 2 indicates a better transient performance. Based on Table 3, the proposed LDO outperforms most of the recent designs. Additionally, the marginal F.O.M.1, improvement over [4] is achieved by using a more cost effective CMOS technology (0.35 μm over 0.13 μm) with doubled $I_{\text{OUT(max)}}$. However, F.O.M.1, 2 of [16] is lower than the proposed design. Besides using advanced 65 nm CMOS which has inherently higher transition frequency $f_T$, $M_{\text{pass}}$ in [16] is much smaller compared to the proposed design, since its $I_{\text{OUT(max)}}$ is only 10 mA.

6. Conclusion

The working concept of the proposed LDO has been proved mathematically and through post-layout simulation that the CMFB resistors and coupling capacitors is able to enhance the $SR_C$. Bandwidth extension is also achieved by ADB technique. The trade-off exhibited by the CMFB resistors is also discussed and the optimum value is selected. Thus, by overcoming the issues of $SR_C$ and bandwidth, the transient response of the proposed LDO is significantly improved while maintaining high current efficiency, keeping the...
power consumption low. Therefore, the proposed LDO is highly recommended for SoC power management implementations.

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References