Voltage dependences of parameter drifts in hot carrier degradation for n-channel LDMOS transistors

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1. Introduction

In recent years, smart power integrated circuits utilizing BCD (Bipolar-CMOS-DMOS) technology have become increasingly popular in the implementation of complex electronics system functions with improved performance, reduced size and lower cost. These multifunction power integrated chips are strongly demanded for the market of portable devices, automotive applications, and display drivers. For many smart-power applications, the capability of handling high drain voltages and high current levels needs to be combined with standard low voltage CMOS logic cells. Lateral DMOS (LDMOS) transistors are the devices of choice and their electrical behavior is well documented. Lateral DMOS transistors are widely used in various smart-power applications, as it can be easily integrated within existing CMOS technologies without significant process changes [1,2]. However, high operational drain and gate biases make the LDMOS devices vulnerable to hot carrier injection (HCI) damage. This has become a serious concern with regard to reliability. Various modified structures have been proposed to improve the trade-off between performance and reliability. One effective way is the utilization of STI in the drift region under the gate end. The STI in the drift region reduces potential crowding and peak electric field under the gate end, a shorter length of the drift region is sufficient to maintain the required drain voltage [1,3]. As the HCI characterization in STI-based LDMOS devices has recently drawn much attention while not many literatures available, it is the motivation of this paper to study the degradation performance for $V_{DS} = 24$ V n-channel LDMOS transistor with STI based structures. This is based on a self-developed device by Malaysia fab for 0.18 μm BCD technology market. Furthermore, very few sets of information are available on the voltage dependences of hot carrier degradation to the parameter drifts for this type of LDMOS. This paper will study the phenomenon and mechanism of HCI $I_{D_{lin}}$ degradation under various $V_{GS}$ and $V_{DS}$ stress range. The test characterization is established using conventional n-channel CMOS HCI test procedure as a reference. Based on experimental data and TCAD simulations result, the mechanisms responsible for the parameter shifts are presented. We demonstrate that different degradation mechanisms occur under these stress conditions.

2. Experimental conditions and methodology

The device used in this research work features an STI in n-drift region near the drain with buried body implant. This device is integrated into a 0.18 μm CMOS compatible process with self-aligned gate on the source side and the drain side. The gate-length and gate-width of the device are 0.4 and 20 μm, respectively. The gate oxide is 11.5 nm. The device operational voltages are at 24 V for $V_{DS}$ and 5 V for $V_{GS}$. The STar Scorpio hiVIP HCE equipment is used to perform hot carrier stress tests. In order to build a comprehensive understanding on voltage bias dependence of hot carrier degradation, a set of DC hot carrier measurements are performed at...
different $V_{GS}$ and $V_{DS}$. The tests are performed at room temperature with the source and substrate connected to ground. The stress is applied until the targeted failure criterion or maximum 100 h are achieved [3,4]. At selected time intervals, the device electrical parameters are measured to monitor the degradation of the device. In this work, the linear current ($I_{D,lin}$ at $V_{DS} = 0.1$ V and $V_{GS} = 5$ V) is the monitoring parameters for the hot carrier stress test. The failure criterion is fixed at maximum 10% of electrical parameter shift [4]. The percent change values are calculated as in Eq. (1).

$$\Delta I_D = \left(\frac{I_D(t) - I_D(0)}{I_D(0)}\right) \cdot 100$$

(1)

This is where $I_D(0)$ is the initial drain current parameter value and $I_D(t)$ is the drain current parameter value at time $t$. The time dependency function describing device degradation under hot carrier stress is the power law [5,6], where the absolute value of the percentage change $\Delta I_D$ in a parameter as a function of time $t$ as in Eq. (2):

$$|Y(t)| = C t^n$$

(2)

Parameter $n$ is considered a technology dependent parameter and parameter $C$ is dependent on technology, temperature and device geometry and stress conditions. This tendency is valid, in particular at short stress times, while at long stress times, the parameter degradation, rather saturate.

In this paper, we use Drain–source voltage acceleration method as in Eq. (3) for lifetime prediction [5]. The simplicity of the Drain–source voltage acceleration model allows quick and easy extrapolation of device lifetime under stressing conditions to the real life basis [5]. The time to reach the failure criteria is obtained by Eq. (3) where $t_0$ and $B$ are fit parameters:

$$t_{ TAR} = t_0 \exp\left(B/V_{DS, stress}\right)$$

(3)

3. Experiment results and discussion

The degradation parameter ($I_{D,lin}$) of LDMOS transistors stressed at various $V_{DS}$ and $V_{GS}$ are shown in Fig. 1(a) and (b). For each voltage stress condition, the linear drain current $I_{D,lin}$ decreases with time and saturates [6]. This is due to the mechanism of interface state generation ($D_A$) and mobility reduction. The $D_A$ occurs in the drift region leading to a decrease in $I_{D,lin}$ [7]. In general, device mobility will be degraded if the interface state density, $N_e$ increases [8] as shown in Eq. (4), where $\mu_0$ represents the bulk mobility [9]:

$$\mu = \mu_0/(1 + aN_e)$$

(4)

As a result, the current decreases and the impact generation will be decreased as well. As the stress time increases, the creation of new interface traps is reduced and the effect of the traps on the current distribution is lessened. Consequently, the degradation mechanism saturates as a certain equilibrium condition is reached. Fig. 1(a) shows the DC hot carrier results for $V_{DS} = 24$ V at different $V_{GS}$ stress. It is observed that the degradation increases with increasing $V_{GS}$ stress, consistent with an expected electron injection mechanism [10]. The impact of $V_{GS}$ on the transistor degradation appears to work in two stages. The first stage is the generation of interface traps and the second stage is the diffusion of traps deeper into the oxide [11]. At lower $V_{GS}$ stress, $V_{GS} < 2.5$ V, the rate at which the interface traps are generated is a strong function of $V_{GS}$. However, at higher $V_{GS}$ stress, $V_{GS} > 2.5$ V, these traps are generated almost instantly with $V_{DS} = 24$ V. As revealed by Aresu et al. [12] this could be attributed to source side electron injection which can be explained by hot electron injection and trapping at the source side of the device. In his study, TCAD simulations of the perpendicular electric field for different $V_{GS}$ stress values were carried out. The result shows that an electric field peak is clearly present at high $V_{GS}$ stress condition at the source of the transistor. The diffusion of traps deeper into the dielectric appears to be almost independent of $V_{GS}$ as both the magnitude and the slope of the degradation appears to converge for all $V_{GS}$ stress voltages [11]. The different in slope indicates the difference in degradation mechanism under high $V_{GS}$ stress and low $V_{GS}$ stress.

Fig. 1(b) shows the DC hot carrier degradation for $V_{DS} = 5$ V at various $V_{GS}$ stress. As $V_{DS}$ is increased, the average energy of the electrons flowing along the Si–SiO2 interface increases. This increases the probability for a colliding electron due to impact ionization, to have sufficient energy to generate interface traps. In contrast to Fig. 1(a), there is no significant variation in the slope value for the three splits of $I_{D,lin}$ degradation before saturation starts to occur at $100$ s of stressing. This shows that the degradation at each voltage stress condition is strongly dependent on $V_{DS}$ and the failure mechanism is similar under different $V_{DS}$ stress. To support the argument in Fig. 1(a) and (b), the time to reach the failure criteria ($t_{TAR}$) for each $V_{GS}$ and $V_{DS}$ stress condition is obtained using Eq. (3) and plotted as in Fig. 2. The $t_{TAR}$ for $V_{GS} = 5$ V at various $V_{DS}$ stress is plotted against exponential $1/V_{DS}$ and the $t_{TAR}$ for $V_{DS} = 24$ V at various $V_{GS}$ stress is plotted against exponential $1/V_{GS}$. The result is almost a linear dependence between the $t_{TAR}$ and exponential $1/V_{DS}$ [13]. This verifies that $V_{DS}$ is an accelerating factor for the hot carrier stress test [6] with $t_0 = 4E – 19$ and $B = 695.6$, respectively. From this graph, $t_0$ is the lifetime of the device when $1/V_{DS} = 0$ or when $V_{DS}$ is very large and the value of $B$ is the slope of the log $t_{TAR}$ vs. $1/V_{DS}$ curve. To understand the degradation mechanisms under various drain and gate voltage stresses, 2D TCAD simulations were carried out and the results analyzed. The simulation results show that when the device is biased at

![Image](102_S.Shahabuddin et al. / Microelectronic Engineering 109 (2013) 101–104)
$V_{DS} = 24\,V$ and $V_{GS} = 5\,V$, two areas of the STI subjected to impact ionization generation are observed. As shown in Fig. 3(a), impact ionization exists at the STI corner closest to the channel and the other one at the STI edge closest to the drain. On the other hand, when the device is biased at lower $V_{GS}$ ($V_{GS} = 1\,V$ and $V_{DS} = 24\,V$ and $20\,V$), only one peak of severe impact ionization exists at the drift region closest to the channel (see Fig. 3(b)). The finding is consistent with the research data by Chen et al. and Rey-Tauriac et al. [1,9]. This indicates that the degradation mechanism differs under various $V_{GS}$ stress, which agrees with the finding in Fig. 1(a). The difference in slope of $I_{D,lin}$ degradation between high $V_{GS}$ stress and low $V_{GS}$ stress in Fig. 1(a) is due to the current path for linear bias point along the Si–SiO$_2$ interface [14]. At high $V_{GS}$ stress, the damage location is along the Si–SiO$_2$ interface. As a result, the $I_{D,lin}$ performance is highly impacted from the beginning of the stress applied. At low $V_{GS}$ stress, the damage is located away from the Si–SiO$_2$ interface. Therefore, the impact of Si–SiO$_2$ hot carrier generates a minimum interface damage at early stage of the stress in comparison to high $V_{GS}$ bias points. This explains the reason why [8] the current degradation is much lower at the beginning of the stress and increases as the stress time increased.

![Fig. 2. $I_D$ device $t_{TAR}$ vs. $1/V_{GS}$ (solid symbol) and $1/V_{DS}$ (open symbol).](image)

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![Fig. 3. (a) TCAD simulation result for $V_{DS} = 24\,V$ and $V_{GS} = 5\,V$ showing the simulated impact ionization rate along the Si/SiO$_2$ interface. (b) Simulated impact ionization rate along the Si/SiO$_2$ interface when the device is biased at $V_{GS} = 1\,V$ and $V_{DS} = 24\,V$ and $20\,V$.](image)

![Fig. 4. Simulated impact ionization rate along the Si/SiO$_2$ interface when the device is biased at fixed $V_{GS}$ and various $V_{DS}$.](image)
In Fig 3(a), the damage created at the region closest to the drain [7] is expected to dominate the drain current degradation, as the damage is much larger. Energetic electron hole pairs are generated because of severe impact ionization generation at this region due to Kirk effect [1,15]. Based on the data in Fig. 3(a) and (b), it is found that the degradation mechanism is highly dependent on the stress voltage at the gate ($V_{GS}$).

Other than that, Fig. 4 shows that at fixed $V_{GS} = 5$ V (high $V_{GS}$ stress), the location of peak impact ionization rate is consistent at various $V_{DS}$ stress. However, the magnitude of the peak impact ionization rate is clearly increased as $V_{DS}$ stress increases. The highest $V_{DS}$ stress produces the greatest impact ionization. The observation from these simulation results verified the influence of $V_{DS}$ as an accelerating factor for the hot carrier stress test. This is consistent with the finding as described in Fig. 2.

4. Conclusions

This paper presents a study of the hot carrier degradation mechanisms for n-channel LDMOS transistor with STI based structures. The slope of $I_{D,lin}$ degradation indicates the different degradation mechanisms under various bias stress conditions. The linear relationship between $t_{ TAR }$ and exponential $1/V_{DS}$ denotes that $V_{DS}$ is an accelerating factor for the hot carrier stress test. The simulation results confirmed the experimental findings. The location of impact ionization differs at various $V_{GS}$ stress but it was found consistent at various $V_{DS}$ stress. The investigations quantified $V_{DS}$ as a significant accelerating factor in the hot carrier stress test. This finding is based on experimental approach performed using STar Scorpio hiVIP HCE equipment and 2D TCAD simulations.

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