A High-conversion Gain, Low-power Mixer Adapting Current Reuse Technique for ZigBee Application

G. H. Tan, M. S. Roslina, H. Ramiah and W. K. Chong

Department of Electrical and Electronic Engineering, University Putra Malaysia, Electrical Engineering, Faculty of Engineering, University of Malaya, Malaysia

ABSTRACT

This paper presents a high-conversion gain, low-power, folded CMOS mixer for ZigBee application in 2.4 GHz of user bandwidth. The proposed mixer adapts current reuse technique to increase the conversion gain while substantially reducing the DC power dissipation. The current from LO stage is reused at the transconductance stage to reduce the power consumption. This mixer is verified in 0.13 \( \mu \)m standard CMOS technology. The simulation result exhibits a high-conversion gain performance (CG) of 10 dB, 1 dB compression point (P1 dB) of \(-13.43\) dBm, third-order intercept point (IIP3) of \(-4.3\) dBm, and a noise figure of 16.67 dB. The circuit draws 675 \( \mu \)A current from the 1.2 V of supply voltage headroom.

Keywords: Complementary metal-oxide semiconductor, Current-reused, High-conversion gain, Mixer, ZigBee.

1. INTRODUCTION

Due to its inherent property of frequency translation, down-converter mixer is an important block in wireless receiver. Significant research output has been reported in low-power implementation catering for the various needs of application, especially in wireless sensor network (WSN) [1]. ZigBee is a specification based on IEEE 802.15.4 regulation which was developed for low-power and low-data rate application such as WSN. This standard operates in the frequency range of 2.4 to 2.4835 GHz with a data rate of 250 kbps and minimum sensitivity requirement of -85 dBm [2,3]. Direct conversion receiver is the preferred choice of adaptation as it saves power, is low in cost, and is suitable for system-on-chip integration [1].

Current bleeding architecture is an intriguing topology for high-performance mixer in the context of linearity and conversion gain enhancement [4]. In the proposed current bleeding topology, the current is branched out in controlling the amount of DC current through the transconductance stage and switching stage, independently. This technique would allow less current to flow through the switching stage and thus reducing the \( C_{gs} \) (gate-source capacitance) of the switching transistors which would substantially increase the switching efficiency [4]. As less current flows through the switching stage, the output load resistance can as well be increased, improving mixer conversions gain [5].

Current-reused bleeding mixer is an alternative of low-power mixer that reuses the current at the bleeding stage to improve its conversion gain [5]. The RF input from the transconductance stage is connected to the input of the bleeding stage to enhance the total transconductance current.

Continuous technology scaling with a proportional voltage headroom reduction outlays a challenge in designing the mixer with limited supply voltage headroom. Folded cascode mixer has been taken to the task to overcome this issue [6]. The switching stage of mixer is folded into the transconductance stage where both switching and transconductance stages run in parallel. This topology will optimize the voltage headroom that a mixer requires to operate [6].

In this paper, a high-conversion gain, low-power mixer is proposed. In this work, the current from the LO switching stage is reused and the signal is ac coupled to the RF transconductance stage to improve its conversion gain. The proposed architecture is simulated in 0.13-m standard CMOS technology. The insights of the mixer architecture and operation are discussed in section 2. The RC-extracted simulation result and analysis are reported in section 3. Finally, the conclusion is drawn in section 4.

2. PROPOSED MIXER

The proposed single balanced mixer is illustrated in Figure 1. The transistors are biased in saturation region. The LO bias current is set to be around 40% of the total current to achieve an optimum conversion gain and noise figure (NF). From the circuit in Figure 1, PMOS
Transistor $M_4$ has been integrated and cascaded between the switching and transconductance stage to improve the LO-RF isolation [7]. $V_y$ is a high-impedance node that is able to provide better isolation between LO and RF port. This transistor also enables the common-mode feedback (CMFB) for the mixer. The mixer output is in negative feedback configuration and would maintain a DC voltage of about 0.65 V across process and temperature variation. Any changes to the DC voltage at the differential output would be sensed at node $V_y$ and reverted back to the input gate of transistor $M_y$, which is configured to be in a CMFB compensation mode to reduce the variation at the output. The AC voltage at the source of transistor $M_y$ will deliver an AC RF current at node $V_y$, which mixes up with the LO switching current.

$$I_{RF} = \left( g_{m3} + g_{m5} \right) \times V_{RF} \times R_{1C} \times g_{m4}$$  (3)

where, $g_{m4}$ is the transconductance for transistor $M_4$ and $I_{RF}$ is the total RF transconductance current before mixing with LO current.

The mixer conversion gain is dependent on the transconductance of transistor $M_4$ and $M_5$, and the output resistance of $R_1$ and $R_2$. Although a significant amount of current is diverted to the transconductance stage, the LO stage bias current is reduced, further encouraging a larger value of resistances $R_1$ and $R_2$. The conversion gain proportionally increases with resistance and is given by:

$$CG = \frac{2}{\pi} \left( \frac{g_{m3} + g_{m5}}{} \right) \times R_{1C} \times g_{m4} \times R_{1,2}$$  (4)

At the IF output, $R_1$-$C_3$ and $R_2$-$C_4$ form a low pass filter, filtering the output high-order mixing spurs. $L_1$ and $C_1$ act as resonators that resonate at 2.4 GHz.

3. SIMULATION AND ANALYSIS OF PROPOSED MIXER

Layout parasitic extraction was executed for the proposed architecture and was validated through Spectre-RF in confirming the enhancement of conversion gain through the current reuse adaptation. AC-coupling capacitor, $C_y$, is removed to eliminate the current reuse adaptation from LO switching stage as a comparative result is presented. The input of transistor $M_4$ and $M_5$ is connected to the RF input and is biased at 0.45 V. In this configuration, no current from LO switching stage will be reused at the transconductance stage. The simulation shows that the conversion gain of 6.35 dB is achieved at an IF frequency of 3 MHz and with a LO power of 0 dBm, as illustrated in Figure 2.

Observing the current-reuse validation, capacitor $C_y$ is integrated between the node $V_y$ and $V_{in}$. The result shows a substantial improvement for conversion gain, indicated to be 10 dB. The conversion gain has improved by 50% when adapting the current reuse from LO switching stage.
High-conversion gain mixer is realized by reusing the current of transistor $M_3$ instead of increasing the current through $M_5$ as in (4). Inherently, transistor $M_4$ exhibits smaller aspect dimension ratio and thus resulting in a smaller gate-drain capacitance, $C_{gd}$ at node $V_y$, resulting in smaller current flow through the LO stage as compared to RF transconductance stage. By reducing the parasitic capacitance at the source node of the switching stage, $V_y$, conversion gain would substantially increase \[8\]. Even though transistor $M_4$ has lower transconductance ($g_m4$), it is able to supply sufficient AC RF current at node $V_y$ resulting from a higher AC voltage at node $V_y$ due to the sum of AC transconductance current of $M_3$ and $M_5$.

Figures 3-5 illustrate the plots of the NF, dynamic range, and linearity of the current reuse mixer, respectively. The NF of the mixer is quite high at about 16.67 dB, but it is acceptable as the noise from mixer will be accumulatively reduced by the gain from the low noise amplifier in the total NF computation for the receiver front-end \[9\].

**Figure 2**: Comparison of CG with and without current-reuse adaption.

**Figure 3**: Simulated NF at IF frequency of 3 MHz.

**Figure 4**: Simulated result of input referred 1 dB compression point.

**Figure 5**: Simulated results of IIP3 with 1 MHz of frequency spacing.
Table 1: Summary results and performance comparison of other mixers

<table>
<thead>
<tr>
<th>Performance parameter</th>
<th>This work</th>
<th>[6]</th>
<th>[9]</th>
<th>[10]</th>
<th>[11]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage (V)</td>
<td>1.2</td>
<td>1</td>
<td>1</td>
<td>2.5</td>
<td>1.5</td>
</tr>
<tr>
<td>Frequency (GHz)</td>
<td>2.4</td>
<td>2.4</td>
<td>2.4</td>
<td>5.1</td>
<td>2.4</td>
</tr>
<tr>
<td>CG (dB)</td>
<td>10</td>
<td>11.9</td>
<td>5.3</td>
<td>9.5</td>
<td>-3.5</td>
</tr>
<tr>
<td>P_{L_{in}} (dBm)</td>
<td>-13.43</td>
<td>-</td>
<td>-7.4</td>
<td>-</td>
<td>-11</td>
</tr>
<tr>
<td>P_{1_{dBm}} (dBm)</td>
<td>-4.3</td>
<td>-3</td>
<td>4.6</td>
<td>-7.5</td>
<td>0</td>
</tr>
<tr>
<td>NF (dB)</td>
<td>16.67</td>
<td>13.9</td>
<td>21.7</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>DC current (mA)</td>
<td>0.67</td>
<td>3.2</td>
<td>3.5</td>
<td>7</td>
<td>1.33</td>
</tr>
<tr>
<td>CMOS technology (µm)</td>
<td>0.13</td>
<td>0.18</td>
<td>0.13</td>
<td>0.18</td>
<td>0.35</td>
</tr>
</tbody>
</table>

CMOS – Complementary metal-oxide semiconductor; NF – Noise figure; CG – Conversion gain; DC – Direct current

The performance summary of the proposed mixer is tabulated in Table 1. In comparison to other recent reported works, the proposed architecture exhibits among the highest conversion gain and lowest current consumption proportionally.

4. CONCLUSION

Low-power current reuse folded mixer was designed and verified in 0.13-µm standard CMOS technology. The current from LO switching stage is reused and folded into the RF transconductance stage to increase the conversion gain by 50% with moderate linearity. The mixer draws 675 µA current from 1.2 V of DC power supply voltage. This architecture has the potential to be scaled to below 1 V of supply to further reduce the power consumption.

REFERENCES


AUTHORS

G. H. Tan received the B.S. and M.S degrees in electronic engineering from University Putra Malaysia in 1999 and 2001, respectively. Currently, he is working toward the PhD degree in University Putra Malaysia, Malaysia. His current research interest includes analogue and Radio Frequency Integrated Circuit Design.

E-mail: tangimheng@yahoo.com

M. S. Roslina received her B.Sc. (Electrical Engineering) degree from George Washington University, Washington D.C, USA, in 1990. She received M.Sc (Microelectronics Systems Design) degree in 1992 and Ph.D degree in 1999 from University of Southampton, UK. She is currently a lecturer in the department of Electrical and Electronic Engineering, University Putra Malaysia. Her research interests include semiconductor devices and IC design.

E-mail: rosolina@eng.upm.edu.my

H. Ramiah received the B.E., M.S., and Ph.D. degrees in electrical and electronics engineering, majoring in analog and digital IC design from University Science Malaysia, Penang, Malaysia, in 2000, 2003, and 2009, respectively. In the year 2003, he was with Sires Labs Sdn. Bhd, Cyberjaya, Malaysia, working on audio pre-amplifier for MEMs ASIC application and the design of 10Gbps optical transceiver solution. In year 2002, he was with Intel Technology Sdn. Bhd., Penang, Malaysia, performing high-frequency signal integrity analysis for high-speed digital data transmission and developing Matlab spread sheet for Eye diagram generation, to evaluate signal response for FCBGA and FCMMAP packages. Currently, he is a Senior Lecturer in the Department of Electrical Engineering, University Malaya. Dr. Harikrishnan was the recipient of Intel Fellowship Grant Award, from 2000 to 2006. His research work has resulted in several technical publications. His main research interest includes Analog Integrated Circuit Design, RFIC Design, and VLSI system design.

E-mail: hrkhari@um.edu.my

W. K. Chong received the B.S. degree in electronic engineering from University Malaysia Perlis, Malaysia, in 2008. Currently, he is working toward the M.S degree in the University of Malaya, Kuala Lumpur, Malaysia. His current research interest includes analogue and Radio Frequency Integrated Circuit Design.

E-mail: wkchong2008@gmail.com