FPGA-Based Pulse-Width Modulation Control
For Single-Phase Multilevel Inverter

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Abstract—Presented is pulse-width modulation (PWM) for single-phase five-level inverter via field-programmable gate array (FPGA). The proposed inverter has conventional full-bridge configuration and one bidirectional switch. The control technique is digitally generated based on multicarrier PWM in Altera DE2 board, which has many features that allow implementation of the system design through Cyclone II FPGA device. A sinusoidal reference signal and two triangular carrier signals in phase and of the same frequency but different offset voltages were used to generate the PWM signals for the inverter switches. Besides Altera Quartus II software, Matlab/Simulink software was used to simulate and verify the proposed circuit before it was implemented in a prototype hardware. Simulation and experiment results closely agreed.

Keywords – Pulse-width modulation (PWM), FPGA, multilevel inverter.

I. INTRODUCTION

Multilevel inverters have been drawing huge interest since recent years, especially in high power and power quality applications. They are advantageous over traditional three-level ones; [1]-[3] near-sinusoidal output waveforms, smaller filter size, lower electro-magnetic interference (EMI), and lower total harmonic distortion (THD) are some of the characteristics that make it popular among researchers and industries.

A multilevel inverter’s output comprises several intermediate voltage levels stepped through. Fig. 1 shows a typical phase-output voltage for three-level and five-level inverters. Generally, there are three common topologies for multilevel inverters: neutral point clamped (NPC) or diode clamped, flying capacitor (FC) or capacitor clamped and cascaded H-bridge (CHB).

The most common modulation methods developed for multilevel inverters are multicarrier pulse-width modulation (PWM), selective harmonic elimination (SHE), and space-vector modulation (SVM). In multicarrier PWM, the carriers can be arranged as follows: phase shifted (PS), phase disposition (PD), phase opposition disposition (POD), or alternate phase opposition disposition (APOD) modulations [1]-[3].

Emergence of field-programmable gate array (FPGA) technology created opportunities for its digital implementation in industrial control system. FPGA technology offers shorter design cycle, much faster computation speed, reduced cost, less-complex circuitry and convenient application in algorithm modification. FPGA-based digital controllers have been successfully used in applications such as PWM inverters [4], multilevel converters [5], power-factor correction [6], and electrical-machine control [7].

This paper presents a single-phase five-level inverter with PWM generator on Altera DE2 board. The output voltage of the proposed inverter can be represented in the following five levels: +Vdc, +½Vdc, zero, -½Vdc, and -Vdc, where Vdc is the magnitude of the dc voltage source. Altera Quartus II software was used to design the PWM pattern in the form of Verilog hardware description language (HDL) and schematic design entry.

II. THE OPERATIONAL OF PROPOSED INVERTER

Fig. 2 shows the proposed inverter’s configuration with LC filter and load resistor [8], [9], modified from conventional full-bridge inverter via addition of an auxiliary bidirectional switch comprising four diodes and one switch S5 connected at dc-source centre. Half levels (positive and negative values) of the PWM output voltages were obtained with proper switching control of the auxiliary bidirectional switch.

The proposed inverter uses a sinusoidal wave as a reference signal (50 Hz) with two triangular carrier signals (20 kHz) to generate the PWM gating signals, as illustrated in Fig. 3 [8]. The carrier waves were in phase and had the same frequency but different offsets. The switching functions were produced by comparing the modulating (reference) signal with the upper and the lower carrier signals.
Table 1 lists the inverter’s switching states. Switches S1, S3, and S5 would be operated at carrier-signal frequency, S2 and S4 to be switched at 50 Hz fundamental frequency. Only two switches would be operated at any one time.

<table>
<thead>
<tr>
<th>S1</th>
<th>S2</th>
<th>S3</th>
<th>S4</th>
<th>S5</th>
<th>Vab</th>
</tr>
</thead>
<tbody>
<tr>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>+Vdc</td>
</tr>
<tr>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>+1/2Vdc</td>
</tr>
<tr>
<td>OFF/</td>
<td>OFF/</td>
<td>OFF/</td>
<td>ON/</td>
<td>OFF/</td>
<td>0</td>
</tr>
<tr>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>-1/2Vdc</td>
</tr>
<tr>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>-Vdc</td>
</tr>
</tbody>
</table>

III. PWM GENERATION VIA FPGA

Control algorithm of the proposed inverter was digitally implemented in an Altera DE2 board. The DE2 board has Cyclone II 2C35 FPGA device as the main feature consists of 33 216 logic elements (LEs), 483 840 total RAM bits, 35 embedded multipliers, 4 PLLs, and 475 user I/O pins. Other features used on the DE2 board are a 50 MHz oscillator for clock source, one pushbutton switch for system reset and five toggle switches for the selection of modulation index values.

Fig. 4 presents the block diagram of a single-phase PWM generator developed in Altera Quartus II software. The Quartus II software is the most comprehensive environment available for an FPGA design. The implementation of PWM generator was done in Verilog HDL and schematic design entry.

Relationship between sampling frequency and carrier frequency is based on Nyquist sampling theorem [10], which states that sampling frequency f_s must be at least twice the analog signal’s highest frequency component. Equation (2) defines the relationship between carrier frequency and sampling frequency,

\[ f_s \geq 2 f_c \]

where f_s is sampling frequency and f_c is carrier frequency.

Carrier frequency for the PWM was set to 20 kHz, whereas controller sampling frequency fixed at 40 kHz met Nyquist theorem’s minimum requirement. The modulating and the carrier signals were sampled at 40 kHz frequency and stored in lookup tables (LUTs). A 50 MHz oscillator on the Altera DE2 board was used to clock the overall system, defined as the main system’s clock frequency f_sys. The system clock was thus divided by k = 1250 to adjust with LUT data count,

\[ k = \frac{f_{sys}}{f_c} \]

where f_sys is the main system clock frequency and f_c is the sampling frequency.
The modulator uses a 90° sine wave LUT and programmed it in RAM. There are \( N = 200 \) data generated for 90° (quarter cycle) of a sine waveform as expressed in (4). Thus, 400 points are represented for one complete half cycle of the sine waveform.

\[
N = \frac{f_s}{4f_{sin}}
\]  

(4)

where \( f_s \) is 40 kHz sampling frequency and \( f_{sin} \) the 50 Hz reference frequency.

The sine-wave data was then multiplied by the amplitude modulation index \( M_a \) to produce the modulating signal. For the upper and the lower triangle waveforms, two data of different magnitudes were stored in the LUT. The upper and the lower carrier signals were compared with the modulating signal to produce the PWM signal.

To prevent a short circuit across the input voltage source, dead-time \( T_{dead} \) was included in the gating signals of the switches at each inverter leg [8]. The dead-time (usually called delay time or blanking time) was relatively short. The magnitude of \( T_{dead} \) was set to 0.2 \( \mu \text{s} \) during switch on and switch off of the PWM, whose response to dead time is shown in Fig. 5.

Fig. 6 illustrates the PWM scheme generator designed in Altera Quartus II software. Three schematic blocks represent frequency divider, pulse generator, and dead-time modules. Fig. 7 shows the Verilog HDL frequency-divider-module design entry for construction of 40 kHz sampling frequency and dead-time.

Fig. 8 depicts the schematic diagram of the sine-wave, carrier waves, modulation index and pulse logic blocks in the pulse-generator module. Fig. 9 shows the register transfer level (RTL) graphic for the pulse-logic module designed for the PWM generator. The Quartus II software lets the designer view the RTL graphic of the design entry. This view most closely represents the system, designed in FPGA.

IV. SIMULATION AND EXPERIMENTAL RESULTS

The proposed inverter’s model was simulated on Matlab/Simulink to verify its operation. Its FPGA-based PWM generator was designed by using Verilog HDL and schematic design entry; simulation was realized in Quartus II software. The PWM pattern was designed for modulation index \( M_a = 0.7 \). Performance of the proposed inverter system with LC filter and load resistor was observed.
Fig. 10 shows the simulation results of the PWM signals from Quartus II and Matlab/Simulink. Fig. 11 depicts the simulation result for the 0.2 $\mu$s dead time design. Fig. 12 gives the experiment results for the PWM switching signals; generated by the DE2 board, they agreed well with those obtained from the Quartus II and Matlab/Simulink simulations.

For simulation purposes, the dc bus voltage is set to 200 V. The proposed inverter was implemented with LC filter where $L_f = 3$ mH, $C_f = 470 \mu$F and the resistive load is 100 $\Omega$. Fig. 13 shows the simulated waveforms of the output voltage before and after filtering. Fig. 14 shows the output voltage and load current waveforms. The PWM switching pattern developed in the Altera DE2 board was tested in a prototype of the proposed inverter, whose performance with LC filter and 0.2 $\mu$s dead-time was observed at modulation index $M_a = 0.7$. Fig. 15 depicts the experiment result for the output voltage waveforms before and after filtering. Fig. 16 shows the experiment result for output voltage and load current waveforms. The simulation and experiment results show that five-level output voltage $V_{AB}$ and
sinusoidal filtered output voltage $V_O$ are identical. The load current $I_L$ is nearly sinusoidal and in-phase with the filtered output voltage $V_O$. Fig. 17 shows the total harmonic distortion (THD) of the filtered ac voltage, the THD being 2.41%.

Figure 14. Simulation result for the output voltage and load current waveforms.

Figure 15. Experiment result for the output voltage waveforms, before and after filtering.

Figure 16. Experiment result for the output voltage and load current waveforms.
PWM switching patterns were applied to the proposed inverter switches to produce a five-level output voltage. Altera FPGA enabled fast, flexible design and implementation. Simulation and experiment results were satisfactory for pulse generation, the five-level output voltage and the filtered output voltage and current.

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